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EXAMINER	
NGUYEN, LEON VIET Q	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,862	WASHAKOWSKI ET AL.	
	Examiner	Art Unit	
	Leon-Viet Q. Nguyen	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1-17 and 20-22* is/are rejected.

7)☒ Claim(s) *18,19 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/5/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 7/5/07. Claims 1-23 are pending on this application.

2. Applicant's amendment overcomes the following objection/rejection:

   a. Objection to claims 3, 12, and 15

   b. Rejection of claims 1-4, 7, 8, 10-13 and 18-21 under 35 USC 102(b)

   c. Rejection of claims 5, 6, 9, 14, 16, 17, 22 and 23 under 35 USC 103(a)

3. Applicant's arguments, see Remarks pages 8-11, filed 7/5/2007, with respect to the rejection(s) of claim(s) 1-23 have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ben-Eli (US6873661), Young et al (US5570392), Blomenkamp (US3959586), Glas et al (US6560296B1), Clark et al (US4736362), Iwamatsu et al (US5648988), and Stanley et al (US20020141440).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 5, 7, 8, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Ben-Eli (US6873661).

Re claim 1, Ben-Eli discloses a method for shaping a baseband signal comprising:

providing a plurality of coefficient memories (LUT 20 and 20' in fig. 3, col. 3 lines 49-50), each having a plurality of coefficients values representing filter response waveform values (col. 1 lines 55-64, col. 6 lines 27-28);

determining a coefficient memory address for each of the coefficient memories (col. 8 lines 57-67);

addressing each of the plurality of coefficient memories (col. 8 lines 57-67);

retrieving an addressed coefficient value from each of the plurality of coefficient memories (col. 6 lines 1-2, col. 9 lines 1-3, it is inherent that values of LUT 20 and 20' be retrieved so that they can be added together);

providing a negative value for each of the retrieved ones of the plurality of coefficient values (2's complement units 24 and 24' in fig. 3, col. 6 lines 19-26);

selecting in response to the baseband signal for each coefficient value (col. 8 lines 47-51), one of the retrieved coefficient value and the negative value (fig. 3, it is inherent that the inputs to Muxes 21 and 21' would be the coefficient value from LUTs 20 and 20' and the negative value from 2's complement units 24 and 24' respectively); and

summing the selected value from each coefficient memory for providing a shaped signal (col. 6 lines 7-9, col. 9 lines 1-3).

Re claim 2, Ben-Eli discloses a method of further comprising sharing the plurality of coefficient memories (col. 7 lines 58-60) for shaping both an in-phase baseband signal and a quadrature baseband signal (fig. 3, it is well known in the art that modulators operate to shape a data signal).

Re claim 5, Ben-Eli discloses a method wherein determining a coefficient memory address comprises:

determining an increment for providing a predetermined number of samples for each of a plurality of symbols comprising the baseband signal (col. 3 lines 42-45, it is inherent that the increment be determined before successfully incrementing the address); and

incrementing an address counter (col. 3 lines 42-43) in response to the predetermined number of samples for each symbol (col. 3 lines 43-45) and a predetermined coefficient memory size (col. 7 lines 28-48).

Re claim 7, Ben-Eli discloses a method wherein the negative value (the output of 2's complement units 24 and 24' in fig. 3) comprises at least one of:

a 2's complement value (2's complement units 24 and 24' in fig. 3, col. 6 lines 25-26);

an offset binary value; and

a signed magnitude value.

Re claim 8, Ben-Eli discloses a method wherein providing a plurality of coefficient memories comprises combining at least two filter coefficients (fig. 3, col. 7 lines 53-54. The coefficient value and 2's complemented inverted value are combined) for forming the plurality of coefficient values such that coefficient memory storage is minimized (col. 7 lines 54-56).

Re claim 10, Ben-Eli discloses a method wherein the plurality of coefficient memories further includes one of:

the sum of a first filter response value and a second filter response value (col. 1 lines 50-60,col. 5 lines 66-67. V_i is interpreted to be the sum of the outputs of an FIR digital filter, which is a filter response value); and

the difference of a first filter response value and a second filter response value; and

wherein the step of retrieving an addressed coefficient value retrieves one of the sum of a first filter response value and a second filter response value and the difference of a first filter response value and a second filter response value (col. 6 lines 1-2, col. 9 lines 1-3, it is inherent that values of LUT 20 and 20' be retrieved so that they can be added together).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 4, 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Eli (US6873661) in view of Young et al (US5570392).

Re claim 3, Ben-Eli fails to teach a method wherein sharing the plurality of memories comprises:

retrieving one of the coefficient values corresponding to the in-phase baseband signal on a first edge of a clock signal; and

retrieving one of the coefficient values corresponding to the the quadrature baseband signal on a different second edge of the clock signal.

However Young teaches a method wherein sharing the plurality of memories comprises:

retrieving one of the coefficient values corresponding to the in-phase baseband signal (col. 17 lines 45, c_0 is the coefficient value and $v_I(m)$ is the in-phase signal) on a first edge of a clock signal (col. 17 line 45, clock 0 is the first cycle/edge of the clock signal); and

retrieving one of the coefficient values corresponding to the quadrature baseband signal (col. 17 lines 49-51, c_4 is the coefficient value and $v_Q(m+4)$ is the quadrature

signal) on a different second edge of the clock signal (col. 17 line 49, clock 1 is the second cycle/edge of the clock signal).

Therefore taking the combined teachings of Ben-Eli and Young as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of Young into the method of Ben-Eli. The motivation to combine Young and Ben-Eli would be to separate the I and Q signals without loss of information (col. 17 lines 13-16).

Re claim 4, the modified invention of Ben-Eli teaches a method wherein the clock signal comprises a digital to analog converter clock signal (col. 1 lines 41-50, the signal is converted from analog to digital then reconstructed to an analog signal). Furthermore, it is well known in the art that a digital to analog converter has a clock signal to control the sampling rate.

Re claim 11 Ben-Eli fails to teach a method wherein the first filter response and the second filter response are symmetric.

However Young teaches a method wherein the first filter response and the second filter response are symmetric (col. 16 lines 12-15).

Therefore taking the combined teachings of Ben-Eli and Young as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of Young into the method of Ben-Eli. The motivation to combine Young and Ben-Eli would be to separate the I and Q signals without loss of information (col. 17 lines 13-16).

Re claim 12, Ben-Eli fails to teach a method wherein retrieving coefficient values comprises:

providing an address counter having a plurality of logic outputs for addressing the coefficient memories; and

determining whether to retrieve one of the sum of a first filter response value and a second filter response value and the difference of a first filter response value and a second filter response value in response to selected ones of the logic outputs.

However Young teaches a method wherein retrieving coefficient values comprises:

providing an address counter (326 and 330 in fig. 3) having a plurality of logic outputs for addressing the coefficient memories (col. 18 lines 48-59, it is disclosed in fig. 2 of US5440506 is that the address generators coupled to RAM and ROM are the same); and

determining for each coefficient memory whether to retrieve one the sum of a first filter response value and a second filter response value and the difference of a first filter response value and a second filter response value in response to selected ones of the logic outputs (col. 16 lines 12-16, selecting the sum and coefficient values addressed by the address generator to be multiplied together).

Therefore taking the combined teachings of Ben-Eli and Young as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of Young into the method of Ben-Eli. The motivation to combine Young and Ben-Eli would be to separate the I and Q signals without loss of information (col. 17 lines 13-16).

Re claim 13, the modified invention of Ben-Eli teaches a method further comprising:

providing a logic circuit (322 in fig. 3 of Young) having an output, a first input coupled to a logic output of the address counter (the output of 326 to 322 in fig. 3 of Young), a second input coupled to an in-phase data symbol bit (col. 19 lines 10-11 of Young) and a third input coupled to a quadrature data symbol bit (col. 19 line 12 of Young);

determining whether to select one of the retrieved value and the negative value in response to the output of the logic circuit (col. 19 lines 22-23 of Young, it is obvious to

one of ordinary skill in the art that one of the coefficient values corresponding to the inputs is selected for reading and writing).

Re claim 14, Ben-Eli fails to teach a method wherein summing the selected value comprises:

providing a plurality of adder stages, each adder coupled to a pipeline register;

clocking the pipeline register at a digital to analog converter (D/A) rate; and scaling and formatting the summed values after a final adder stage.

However Young teaches a method wherein summing the selected value comprises:

providing a plurality of adder stages (808, fig. 9, col. 8 lines 15-17), each adder coupled to a pipeline register (fig. 8);

clocking the pipeline register at a digital to analog converter (D/A) rate (Young does not explicitly state using the D/A rate. However it would have been obvious to one of ordinary skill in the art to use the rate of the D/A converter in lines 41-50, which decreases the sampling rate without loss of information, to clock the registers); and scaling and formatting the summed values (341) after a final adder stage (810). It is noted that Young discloses a standard multiplier design in fig. 8, which is taken to be the equivalent of the multipliers 332 and 333.

Therefore taking the combined teachings of Ben-Eli and Young as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of Young into the method of Ben-Eli. The motivation to combine Young and Ben-Eli would be to separate the I and Q signals without loss of information (col. 17 lines 13-16).

8. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Eli (US6873661) in view of Glas et al (US6560296B1).

Re claim 6, Ben-Eli fails to teach a method wherein the baseband signal comprises an in-phase signal and a quadrature signal;

wherein selecting for each coefficient value comprises selecting an in-phase value in response to the in-phase and selecting a quadrature value in response to the quadrature signal; and

wherein summing the selected values comprises summing the selected in phase values for providing a shaped in phase signal, and summing the selected quadrature for providing a shaped quadrature signal.

However Glas teaches a method wherein the baseband signal comprises an in-phase signal and a quadrature signal (fig. 6);

wherein selecting for each coefficient value comprises selecting an in-phase value in response to the in-phase signal (col. 4 lines 23-26, a response from the in-

phase digital data signal combined with the oscillator is expected) and selecting a quadrature value in response to the quadrature signal (col. 4 lines 23-26, a response from the quadrature-phase digital data signal combined with the oscillator is expected); and

wherein summing the selected values comprises summing the selected in phase values (fig. 6, CEI1 and CEI2 summed together in 20) for providing a shaped in phase signal (I-RF OUT), and summing the selected quadrature (fig. 6, CEQ1 and CEQ2 summed together in 20) for providing a shaped quadrature signal (Q-RF OUT).

Therefore taking the combined teachings of Ben-Eli and Glas as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of combining I and Q signals of Glas into the method of Ben-Eli. The motivation to combine Glas and Ben-Eli would be to perform QPSK modulation (col. 2 lines 46-47) which requires half the bandwith of BPSK modulation (col. 1 lines 46-47) and therefore increasing efficiency.

9. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Eli (US6873661) in view of Iwamatsu et al (US5648988).

Re claim 9, Ben-Eli fails to teach a method wherein providing the plurality of coefficient memories provided further provide coefficient values corresponding to a plurality of roll-off factors. However Iwamatsu teaches first and second memory devices

(col. 2 lines 63-67) that comprise of tap rating ratios output to roll-off filters (col. 2 line 62-col. 3 line 6).

Therefore taking the combined teachings of Ben-Eli and Iwamatsu as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the memory devices of Iwamatsu into method of Ben-Eli. The motivation to combine Iwamatsu and Ben-Eli would be to detect a location of a cause of deterioration of pulse forms (col. 3 lines 11-12) and provide for pulse shaping.

10. Claims 16-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Eli (US6873661) in view of Stanley et al (US20020141440).

Re claim 16, Ben-Eli fails to teach a method wherein the filter waveform comprises a raised cosine. However Stanley teaches a low-pass finite impulse response filter with a square-root raised cosine response (¶0103). It would have been obvious and necessitated to use a raised cosine filter.

Therefore taking the combined teachings of Ben-Eli and Stanley as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the filter of Stanley into the method of Ben-Eli. The motivation to combine Stanley and Ben-Eli would be to reduce inter-symbol interference (¶0103).

Re claim 17, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 16.

11. **Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Eli (US6873661) in view of Blomenkamp (US3959586) and further in view of Clark et al (US4736362).**

Re claim 20, Ben-Eli teaches a device comprising:

a plurality of coefficient memories (LUT's 20 and 20' in fig. 3), each memory having an input address bus (the output of counter 17 to LUT's 20 and 20' in fig. 3), a multiplexor input (the outputs of multiplexors 115, 116, 117, and 118 to LUT's 20 and 20' in fig. 3) and a coefficient value output (the output of LUT's 20 and 20' in fig. 3);

a plurality of first registers (registers 53 and 54 in fig. 3, col. 5 lines 35-38. Ben-Eli suggests that the two sections could be structurally separated, which would result in two registers), each having an input coupled to a respective one of the coefficient value outputs (the input to registers 53 and 54 coupled to the output of LUT's 20 and 20' in fig. 3) and an output (the input to registers 53 and 54 in fig. 3);

a plurality of negative value circuits (2's complement units 120-123 in fig. 3), each circuit having an input coupled to a respective one of the first register outputs (the output of registers 53 and 54 coupled to 2's complement units 120-123 in fig. 3), and an output (the output of 2's complement units 120-123 in fig. 3);

a plurality of 2:1 multiplexors (multiplexors 115-118 in fig. 3), each having a first

input coupled to a respective one of the first register outputs (the output from registers 53 and 54 coupled to the input of multiplexors 115-118 in fig. 3) and having a second input coupled to a respective one of the output of the plurality of negative value circuits (the output of 2's complement units 120-123 coupled to the input of multiplexors 115-118 in fig. 3);

and

an adder having a plurality of inputs coupled to respective ones of the plurality of registers (adder 23 in fig. 3).

Ben-Eli fails to teach a digital to analog clock input to the first and second registers and a plurality of second registers, each having an input coupled to a respective one of the outputs of the plurality of 2:1 multiplexors, an output.

Clark et al teaches a multiplexor consisting of three sections, each comprising a plurality of registers (abstract). One of ordinary skill in the art would have found it obvious to use the multiplexor of Clark in place of multiplexors 21 and 21' in fig. 3 of Ben-Eli. Multiplexors 21 and 21' in fig. 3 of Ben-Eli are coupled to the outputs of 2:1 multiplexors 115-118 in fig. 3 of Ben-Eli and each has an output (fig. 3 of Ben-Eli). The motivation to combine Clark and Ben-Eli would be to establish data paths between several possible source and destinations (col. 2 lines 16-19), thus synchronizing various devices.

Blomenkamp teaches clocking a summing and hold circuit (Voltage summing and hold circuit 120 in fig. 21 is interpreted to be a register which stores values) which a digital to analog clock (digital to analog control clock 121 in fig. 21). One of ordinary skill in the art would have found it obvious to use the D/A clock of Blomenkamp to clock registers 53, 54, 21 and 21' in fig. 3 of Ben-Eli. The motivation to combine Blomenkamp and Ben-Eli would be achieve greater information density in a communication line (col. 2 lines 4-8).

Re claim 21, the modified invention of Ben-Eli teaches a device wherein each of the plurality of negative value circuits comprises at least one of: a 2's complement logic element; an offset binary logic element; and a signed magnitude logic element (2's complement units 120-123, 24, and 24' in fig 3 of Ben-Eli).

Re claim 22, the modified invention of Ben-Eli teaches a device further comprising a coefficient address generator (col. 5 lines 51-59, oversampling counter 16 in fig. 3) having an output coupled to a coefficient memory input address bus (fig. 3), the input address having a plurality of address lines (col. 5 lines 51-59, the sample value addresses are interpreted to be a plurality of address lines).

Allowable Subject Matter

12. Claim 15 is allowed.

13. Claims 18, 19, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/
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